What is claimed is:

1. A method for manufacturing capacitor of semiconductor device, the method comprising the steps of:

forming an interlayer insulating film on a semiconductor substrate having a lower structure;

sequentially forming a bonding layer and a hard mask layer on the interlayer insulating film;

etching the hard mask layer, the bonding layer and the interlayer insulating film to form a storage electrode contact hole exposing a predetermined region of the semiconductor substrate for a storage electrode contact;

forming a storage electrode contact plug filling a predetermined depth of the storage electrode contact hole;

forming a barrier metal layer on the entire surface of the semiconductor substrate to fill up the storage electrode contact hole;

planarizing the barrier metal layer using the hard mask layer as an etch stop layer to form a barrier metal layer pattern;

removing the hard mask layer; and

forming a storage electrode contacting the barrier metal layer pattern on the bonding layer.

2. The method according to claim 1, wherein the

bonding layer comprises a alumina layer having a thickness ranging from 50 - 300Å.

3. The method according to claim 1, wherein the hard mask layer comprises a film containing nitrogen and has a thickness ranging from 100 to 500Å.

4. The method according to claim 3, wherein the film containing nitrogen is a film selected from the group consisting of a plasma induced silicon nitride film, a low pressure silicon nitride film, a nitric oxide film and a tantalum nitride film.

5. The method according to claim 1, wherein the barrier metal layer is selected from the group consisting of TiN layer, TiAlN layer and TiSiN layer having a thickness ranging from 1500 - 2000Å.

6. The method according to claim 1, wherein the step of planarizing the barrier metal layer comprises a CMP process using an acidic slurry containing an oxide or an alumina abrasive and having a pH ranging from 2 - 6.

7. The method according to claim 6, wherein the step of removing the hard mask layer is performed using a

phosphoric acid having a temperature ranging from 140 to 180°C.

8. The method according to claim 1, wherein the storage electrode comprises an iridium layer or a platinum layer.